Rangeen Basu Roy Chowdhury

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Education

- **North Carolina State University** — Jan 2014 — October 2016
  Ph.D. Computer Engineering - ***CPU Architecture*** — GPA: 4.0/4.0
  Advisor – Dr. Eric Rotenberg

- **North Carolina State University** — Aug 2011 — Dec 2013
  M.S. Computer Engineering - ***CPU Architecture*** — GPA: 4.0/4.0

- **National Institute of Technology (NIT),** Durgapur, India — Aug 2005 — May 2009
  B. Tech. Electronics & Communication — GPA: 8.05/10.0

Professional Experience

- **CPU Architecture Researcher,** *Intel Corporation***,** Hillsboro, OR — October 2016 — Present
  Manager: *Sebastian Winkel – sebastian.winkel@intel.com*
  - Research hardware and instruction set improvements in x86 CPUs to maintain competitive edge
  - Model, simulate, and analyze novel performance features in Intel's CPUs
  - Define and document new microarchitectural features
  - Work with designers towards successful implementation of features

- **Research Assistant,** *NC State University,* Raleigh, NC — August 2012 — August 2016
  - **Ph. D. Research:**
    - The goal of my research was to design **an adaptive CPU** named **AnyCore**. AnyCore can dynamically tune its active resources to better suit the workload, and improve performance while optimizing power consumption. In my dissertation, I examined the overheads of AnyCore and presented various comparative analyses. An AnyCore prototype, code named AnyCore-1, was taped out using **IBM 130 nm** process and was successfully validated by us.

    - I was also part of the team responsible for microarchitecture definition, RTL design, and physical implementation of the H3 chip, which is a **3D stacked heterogeneous multi-core processor** with novel microarchitectural techniques for improving single threaded performance. The chip was taped out using **GlobalFoundries 130nm** process and is currently being tested.

  - **Teaching Assistant** for *Computer Design & Technology (ECE521)*, a graduate level computer architecture class.

- **CPU Architecture Intern,** *Nvidia Corporation,* Santa Clara, CA — August 2014 — December 2014
  Manager: *Aravindh Baktha - abaktha@nvidia.com*
  - Post silicon performance and power analysis of **ARM** CPUs
  - Pre-silicon to post-silicon co-relation of benchmarks
  - Develop micro benchmarks to project perf/watt for next generation ARM CPUs

- **Hardware Intern,** *Qualcomm Inc.,* Raleigh, NC — May 2014 — August 2014
  Manager: *Jaya Ganasan – jganasan@qti.qualcomm.com*
  - Power analysis of high performance on-chip interconnect
  - Develop statistical power model of the interconnect

- **CPU Design Intern,** *Nvidia Corporation,* Hillsboro, OR — May 2012 — August 2012
  Manager: *Karol Menezes - kmenzes@nvidia.com*
  - Design and implementation of on chip debug feature**s**
  - Synthesize debug unit to meet timing and area goals

- **R&D Engineer (FPGA),** *Tejas Networks Ltd.,* Bangalore, India — August 2009 — July 2011
  Manager: *Mahesh Prabhu – maheshp@tejasnetworks.com*
  - Design FPGA IPs for M**ulti-gigabit Ethernet Switches, Ethernet over SDH Switches,** and **Memory Controllers**
  - Design chip-to-chip **Multi-gigabit Serial Protocols**
  - On board **Verification** and **Integration** with firmware/software

Publications

- H. Elnawawy, **R. Basu Roy Chowdhury**, A. Awad, G. T. Byrd. *Diligent TLBs: a mechanism for exploiting heterogeneity in TLB miss behavior*. ICS, June 26-28, 2019.

- S. J. Tarsa, **R. Basu Roy Chowdhury**, J. Sebot, G Chinya, J. Gaur, K. Sankaranarayan, CK. Lin, R. Chappell, R. Singhal, H. Wang. *Post-Silicon CPU Adaptations Made Practical Using Machine Learning*. ISCA, June 22-26, 2019.

- V. Srinivasan, **R. Basu Roy Chowdhury**, E. Forbes, R. Widialaksono, Z. Zhang, J. Schabel, S. Ku, S. Lipa, E. Rotenberg, W. Rhett Davis and P. Franzon. H3 (Heterogeneity in 3D): *A Logic-on-logic 3D-stacked Heterogeneous Multi-core Processor.* ICCD, November 5-8, 2017.

- S. Ku, E. Forbes, **R. Basu Roy Chowdhury**, E. Rotenberg. *A Case for Standard-Cell Based RAMs in Highly-Ported Superscalar Processor Structures.* ISQED, March 13-15, 2017.

- R. Widialaksono, **R. Basu Roy Chowdhury,** Z. Zhang, J. Schabel, S. Lipa, E. Rotenberg, W. R. Davis, and P. Franzon. *Physical Design of a 3D-stacked Heterogeneous Multi-Core Processor*. 3DIC-2016, Nov 9-11, 2016.

- **R. Basu Roy Chowdhury,** A. Kannepalli, and E. Rotenberg. *AnyCore-1: A Comprehensively Adaptive 4-way Superscalar Core.* Poster session of Hot Chips 2016, August 21-23, 2016.

- **R. Basu Roy Chowdhury**, A. Kannepalli, S. Ku, E. Rotenberg. *AnyCore: A Synthesizable RTL Model for Exploring and Fabricating Adaptive Superscalar Cores.* ISPASS 2016, April 17-19 2016.

- E. Forbes, Z. Zhang, R. Widialaksono, B. Dwiel, **R. Basu Roy Chowdhury**, V. Srinivasan, S. Lipa, E. Rotenberg, W. R. Davis, and P. D. Franzon. *Under 100-cycle Thread Migration Latency in a Single-ISA Heterogeneous Multi-core Processor.* Poster session of Hot Chips 2015, August 23-25, 2015.

- E. Forbes, **R. Basu Roy Chowdhury**, B. Dwiel, A. Kannepalli, V. Srinivasan, Z. Zhang, R. Widialaksono, T. Belanger, S. Lipa, E. Rotenberg, W. R. Davis, and P. D. Franzon. *Experiences with Two FabScalar-based Chips.* 6th Workshop on Architectural Research Prototyping (WARP'15), in conjunction with ISCA-42, June 14, 2015.

- E. Rotenberg, B. Dwiel, E. Forbes, Z. Zhang, R. Widialaksono, **R. Basu Roy Chowdhury**, N. Tshibangu, S. Lipa, W. Rhett Davis and P. Franzon. *Rationale for a 3D Heterogeneous Multi-core Processor.* Proceedings of the 31st IEEE International Conference on Computer Design (ICCD-31), pp. 154-168, October 2013.

Academic Projects Executed

- **Improving PARSEC performance in a 3D stacked architecture:** Used ***GEM5*** to implement a novel architectural technique to improve performance of some of the benchmarks in the PARSEC benchmark suite.
- **Process Scheduler:** Implemented a Linux like process scheduler in ***Xinu for x86.***
- **Demand Paging:** Implemented demand paging and backing store mapping in ***Xinu for x86.***
- **Low power multi-gigabit off chip transceiver design:** Custom designed a very low power transceiver for off chip communications using current mode logic and equalization.
- **Perf-power optimizations for ARM CPUs:** Optimized embedded software to improve performance and reduce energy
- **Virtualization for CUDA:** Developed a virtualization mechanism for ***CUDA*** applications to allow sharing ***GPU*** resources between Virtual Machine Instances.
- **Compiler Passes:** Developed passes for GCM, CSE and Software Fault Tolerance.
- **FabScalar:** Porting ***OpenSPARCT2*** memory hierarchy to work with a library of configurable superscalar cores.
- **Shared Memory Processor (SMP) Cache Simulator:** Developed trace driven SMP memory hierarchy simulator. Traces were generated using a system simulator.
- **Cache Simulator:** Developed a multilevel memory hierarchy simulator for a course project.

Technical Skills

- **Computer Architecture, Microarchitecture, Power Analysis, Digital Design, Design Automation**
- **Languages :** C++, C, CUDA, Verilog, VHDL, Java, Perl, Python, Shell scripting
- **Tools :** GEM5, FabScalar, McPatt, Synopsys Design Compiler, Prime Time, Cadence NC Sim, SOC Encounter, Cadence Virtuoso, Calibre, Synplify, Xilinx ISE,
- **Computing :** Linux, Office suite, HTML, PHP, JSP, CSS, JavaScript

Accolades

- **Top 0.1% in AISSE**: Was awarded the certificate of merit for being among the top 0.1% of successful candidates of All India Secondary School Examination (10^{th} Grade) 2003 in Science
- **ACM SIGARCH Student Travel Grant** for travel to ISCA 2015

Involvement in Professional Associations

- Member of **IEEE** and **Tau Beta Pi**
- **Officer** for the *ECE Graduate Student Association (GSA)* and department liaison at the University GSA
- Member of organizing committee for Mukti (FOSS symposium) and Motorzundung (Auto Fest) at NIT Durgapur