AnyCore: A Synthesizable RTL Model for Exploring and Fabricating Adaptive Superscalar Cores

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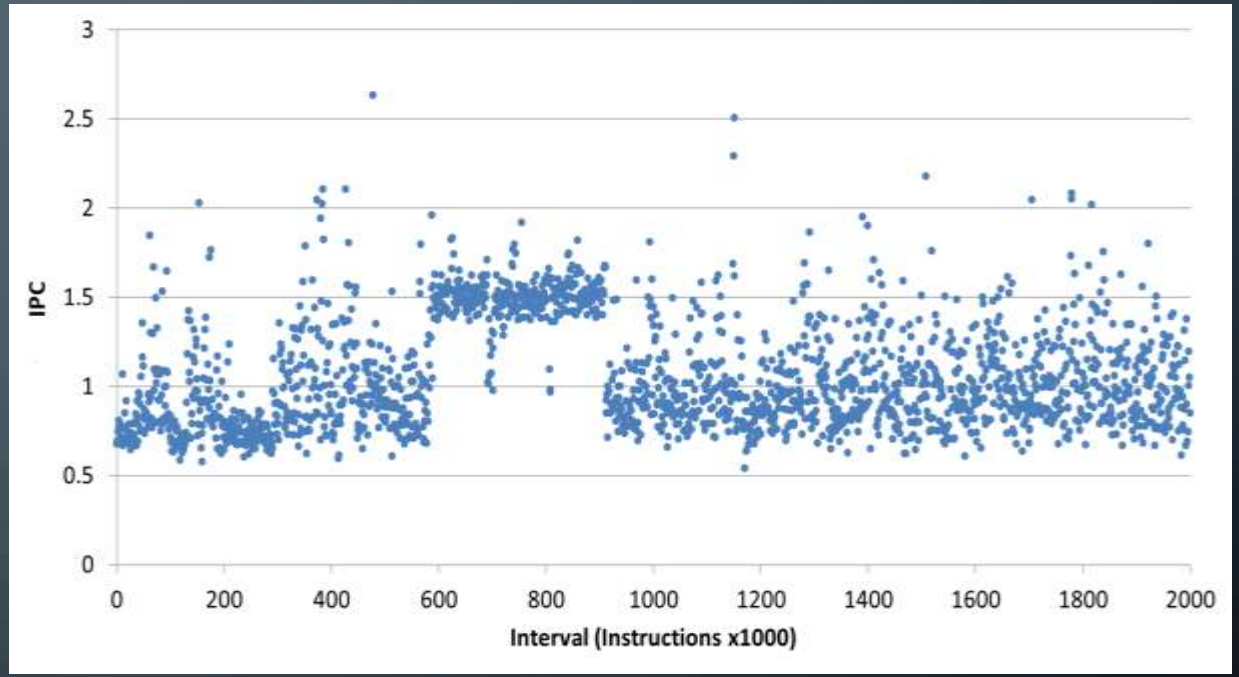
OPPORTUNITY

- Different applications have different amounts of ILP
- Phases of a single application exhibit diverse instruction-level behavior
  - Different amounts of ILP (data dependencies, branch mispredictions)
  - Nearby vs. distant ILP
  - MLP



***Key Point*:** Both coarse-grain and fine-grain variations exist

*Eliott Forbes PhD thesis

PROCESSOR SPECIALIZATION

- Adapt the microarchitecture to these coarse-grain and fine-grain variations
  - Fetch and execution widths
  - Out-of-order window (ROB, PRF, LQ/SQ, IQ)
  - Cache and predictor sizes
  - Pipeline depth
- Two main ways of adapting microarchitecture
  - Heterogeneous multicore
    - Multiple cores with same ISA but different microarchitectures
  - Adaptive
    - Design a single, large core
    - Downsize resources when they're not profitable

OUTLINE

- AnyCore toolset
  - RTL
  - CAD Flow
  - PAT Tool
- Overhead analysis of adaptive cores
- Comparative study of adaptive core vs. heterogeneous multicore
- AnyCore chip

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ANYCORE TOOLSET

- Logic overheads of adaptive core erode its benefits w.r.t. one or multiple fixed cores
- Neglected aspect in adaptive core research
- AnyCore Toolset enables exploring this important aspect

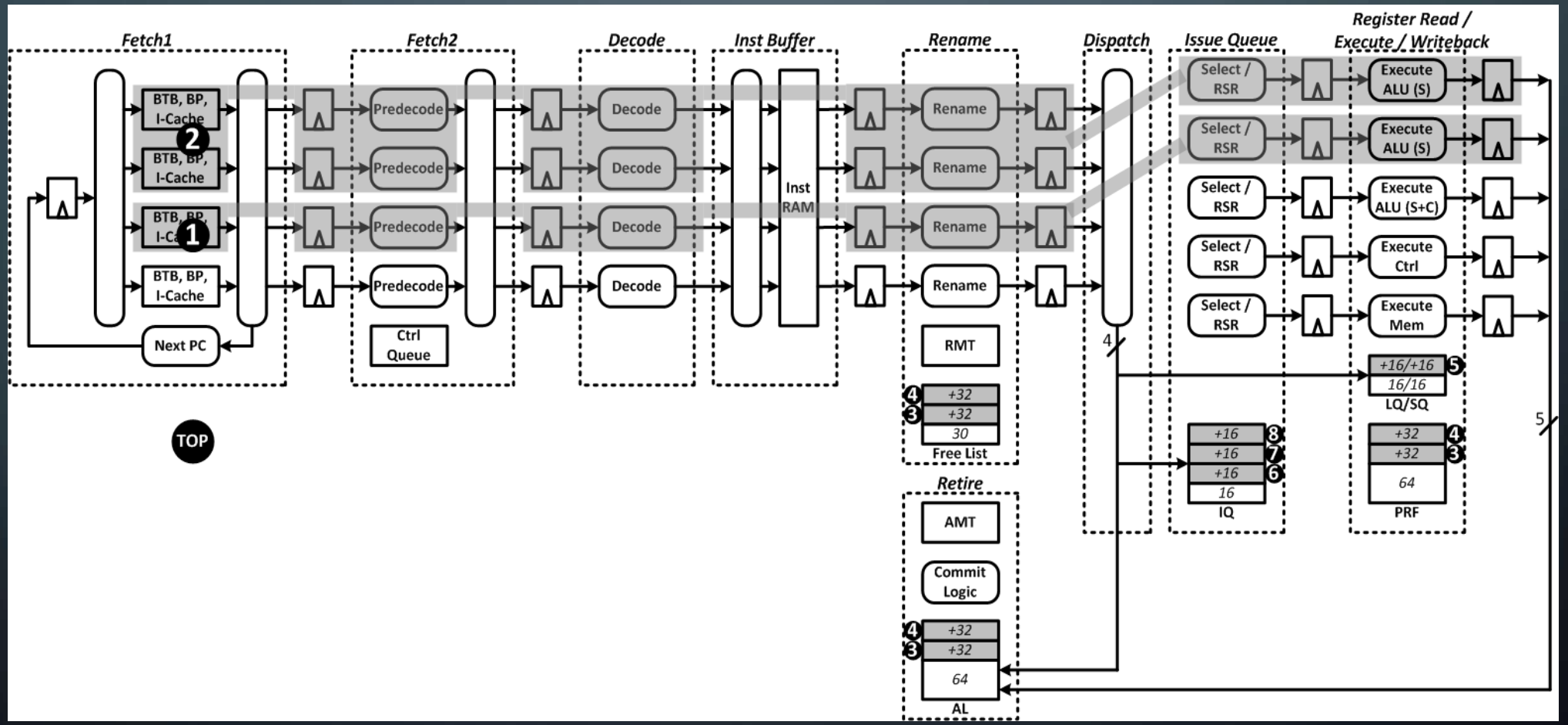
CONTRIBUTIONS OF ANYCORE

- Toolset
  - A synthesizable parameterized RTL design
  - AnyCore PAT tool for architectural studies
- Understand circuit-level overheads of adaptivity
- Compare adaptive core vs. heterogeneous multicore
- Fabricate adaptive superscalar cores

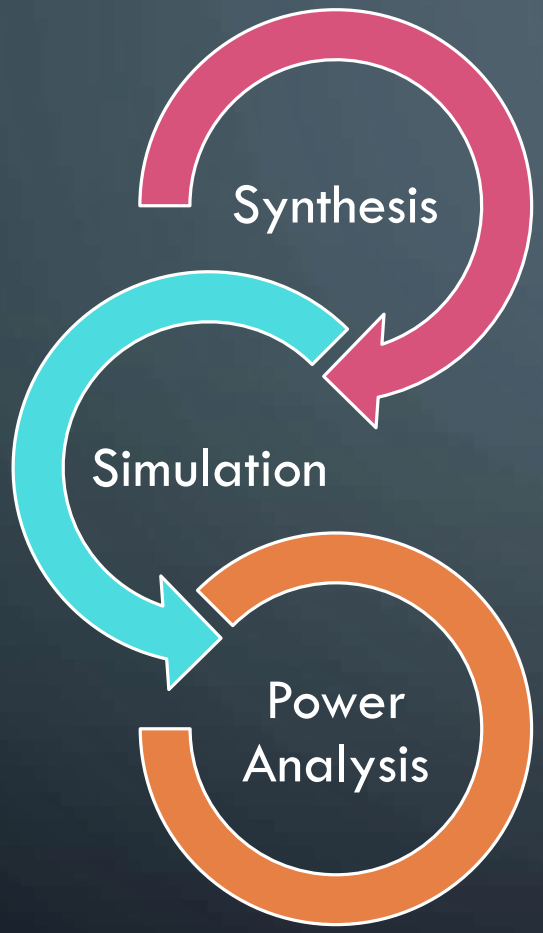
ANYCORE TOOLSET: RTL

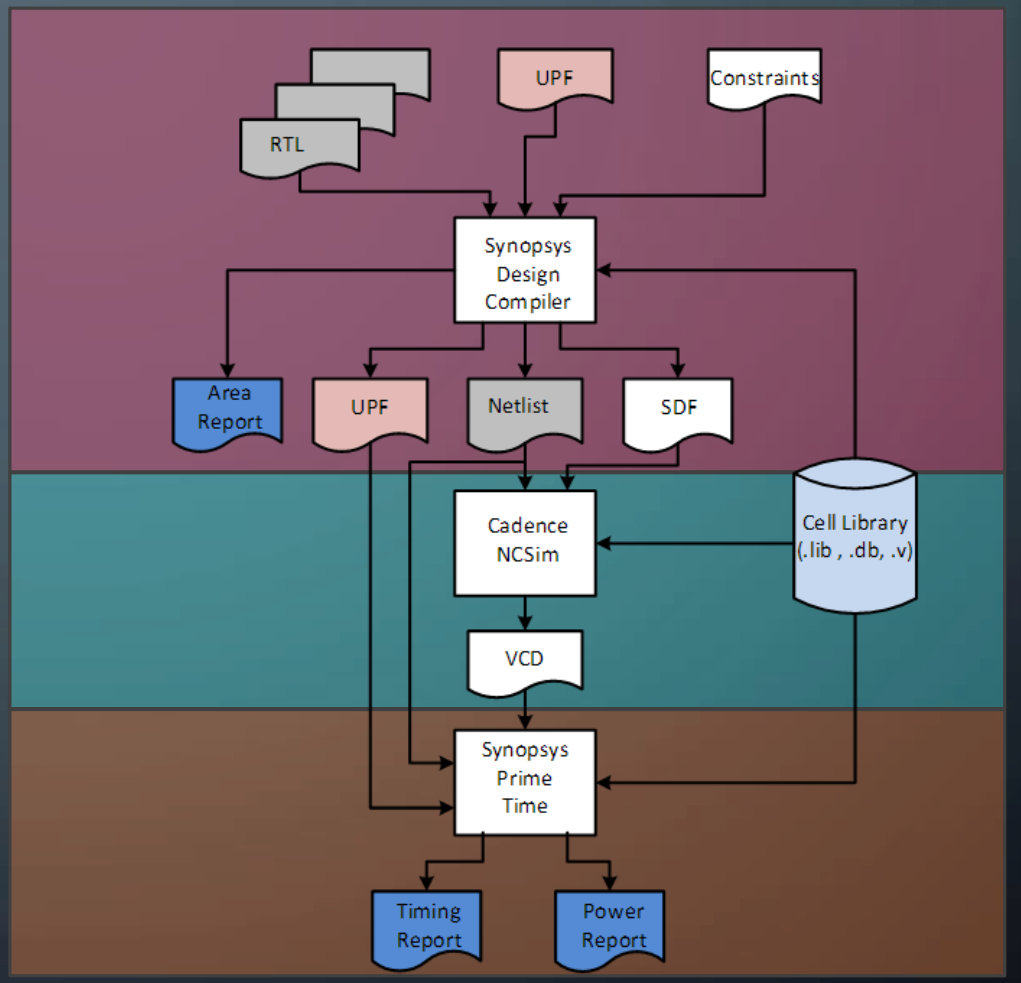
- Three dimensions of parameterization
  - Fixed core or adaptive core
  - Maximum structure sizes, widths, and depths
  - Granularity of adaptivity (for adaptive core)
- Easily excise the adaptivity to build a fixed core
- Many different AnyCore designs can be composed
- Paired with UPF for power gating of partitions

EXAMPLE ANYCORE DESIGN



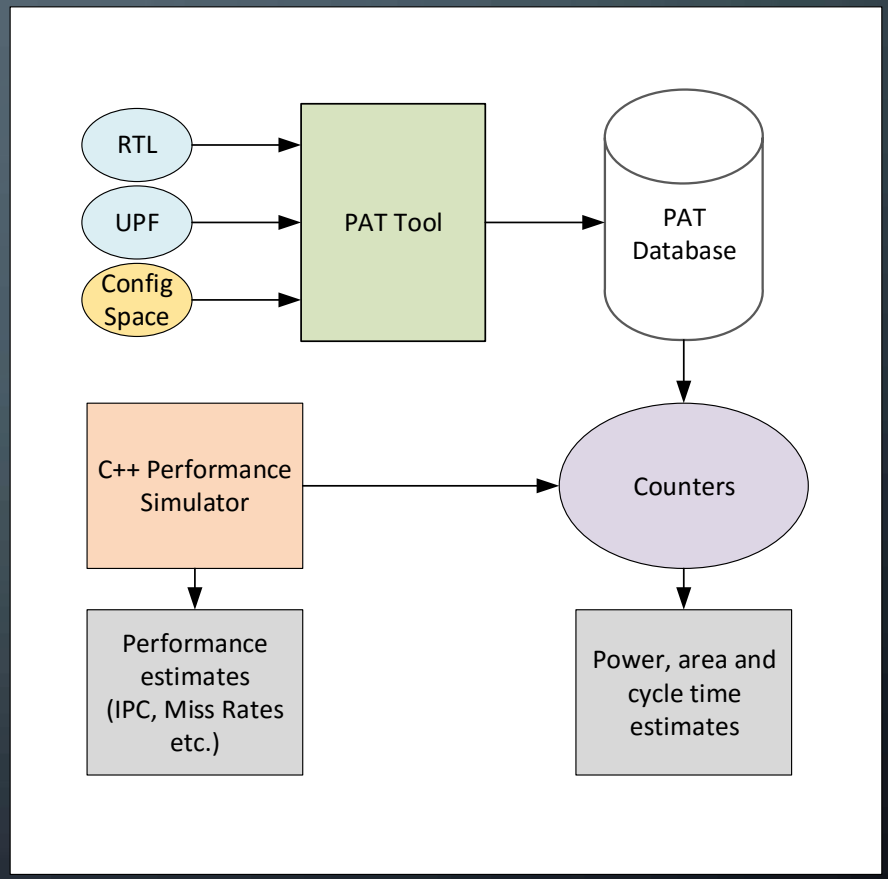
ANYCORE TOOLSET: CAD FLOW





ANYCORE TOOLSET: PAT TOOL

- Power, area and timing estimation tool
- Automated synthesis and analysis flow for populating the PAT Database
- Allows high level architectural exploration when coupled with a performance simulator



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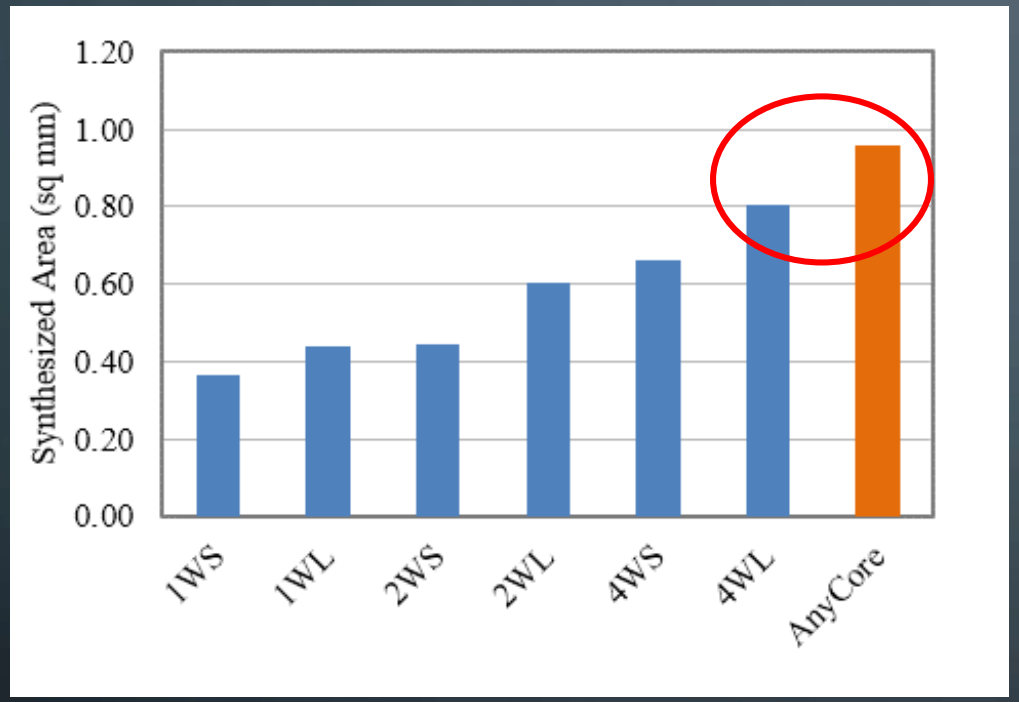
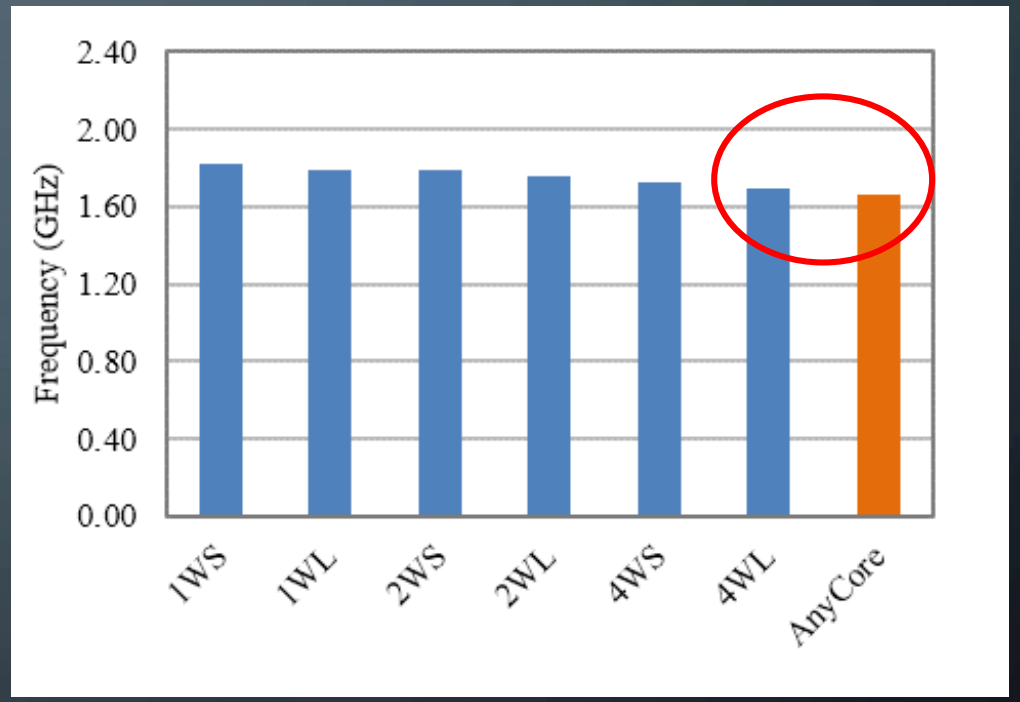
AREA & FREQUENCY

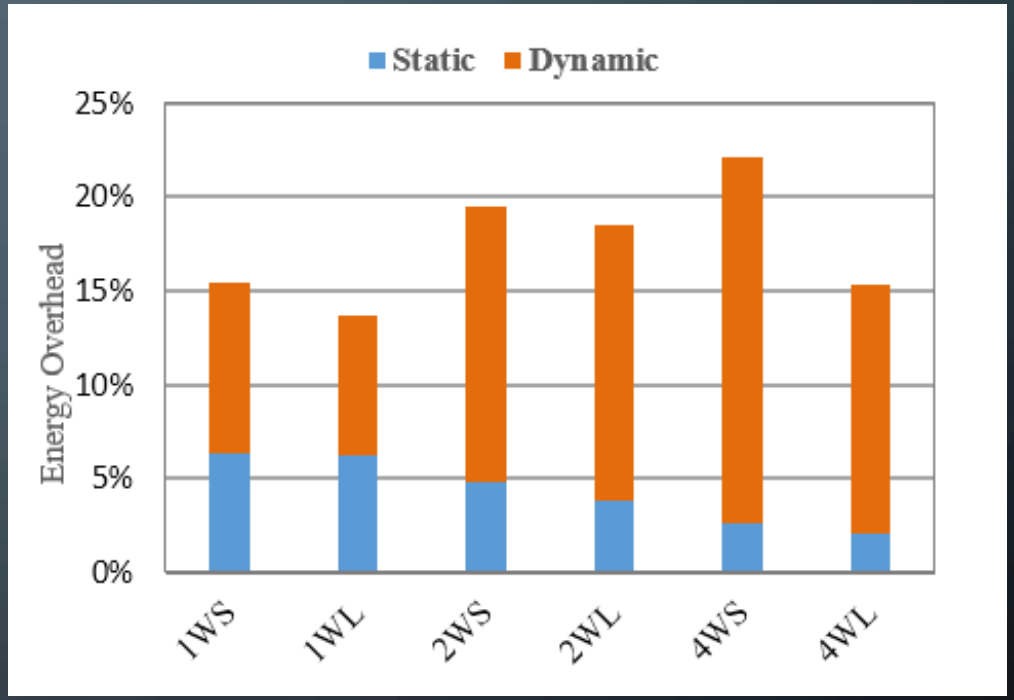




Key point: 19% extra area and 1.67% lower frequency

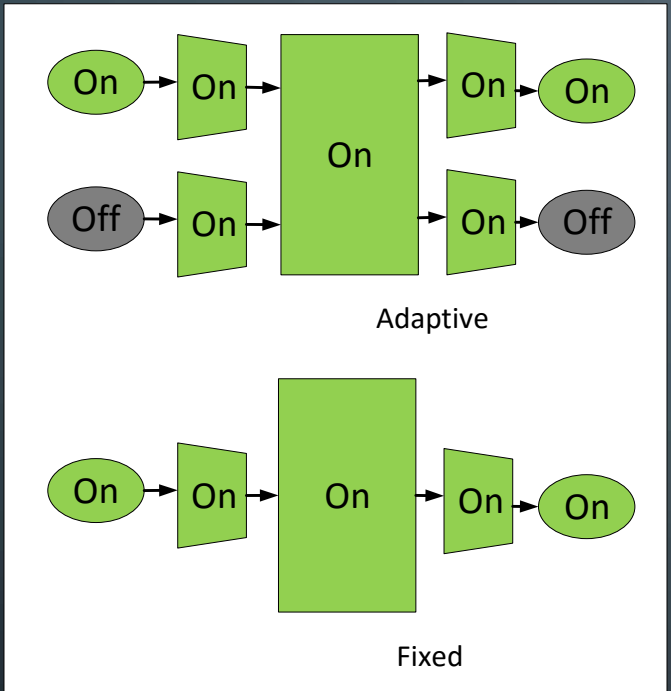
Sources of overhead: Isolation cells, sub-optimal synthesis due to partitioning, input gating, control logic

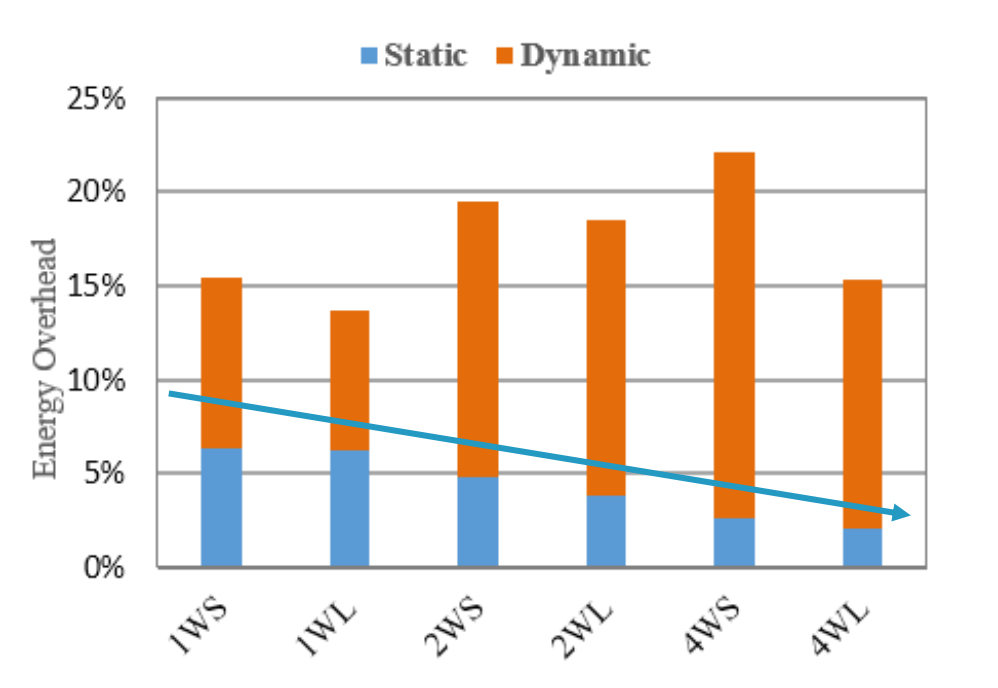
ENERGY



Key point: Adaptive cores have non-negligible overheads largely ignored in previous works

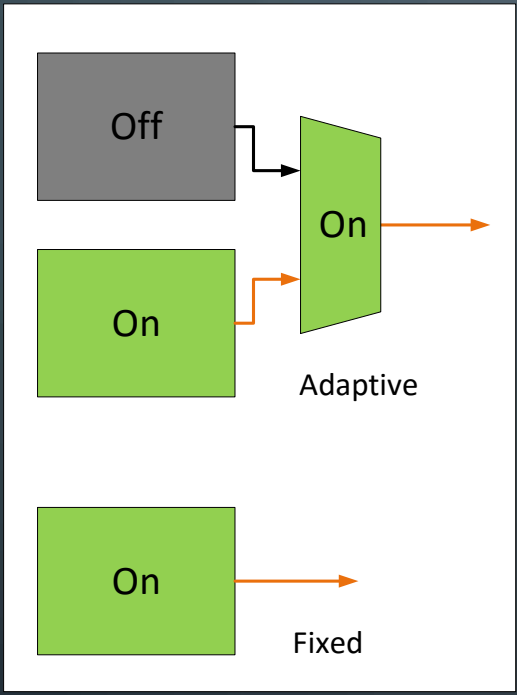
ENERGY

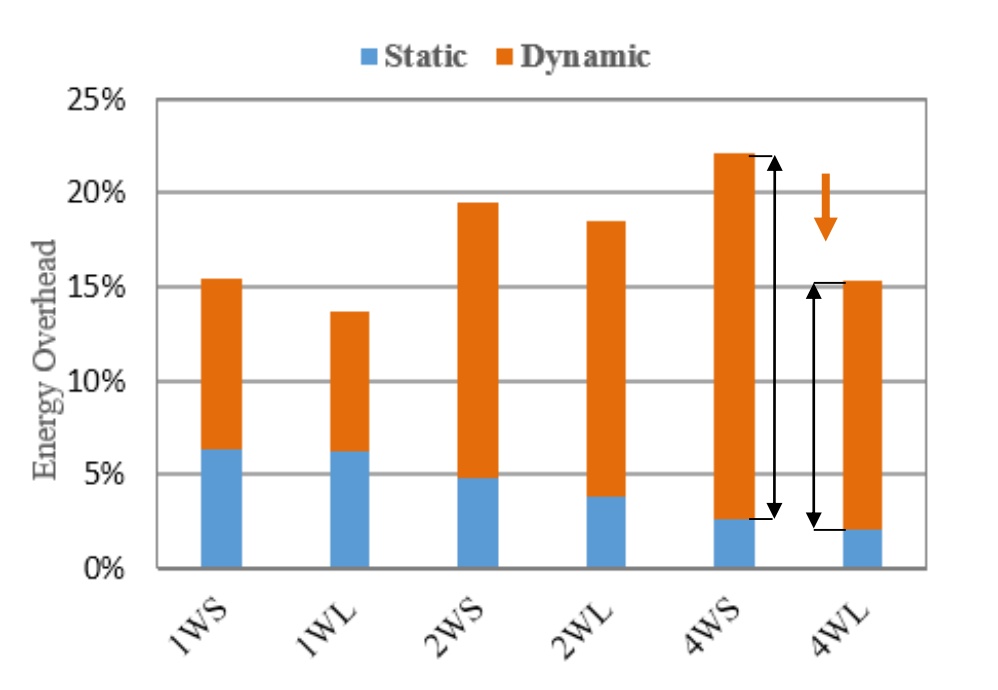




Key Point: Static energy overhead is primarily due to excess static energy of extra ports and excess leakage due to larger cycle time

ENERGY





Key Point: Dynamic Energy Overhead is due to extra muxes for size adaptivity and additional control logic

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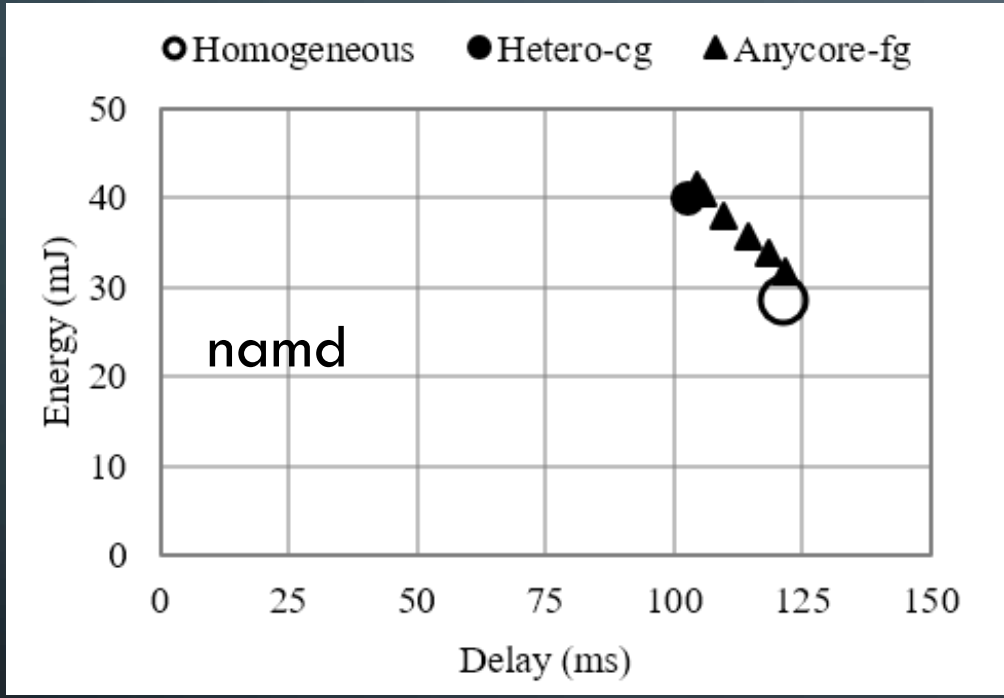
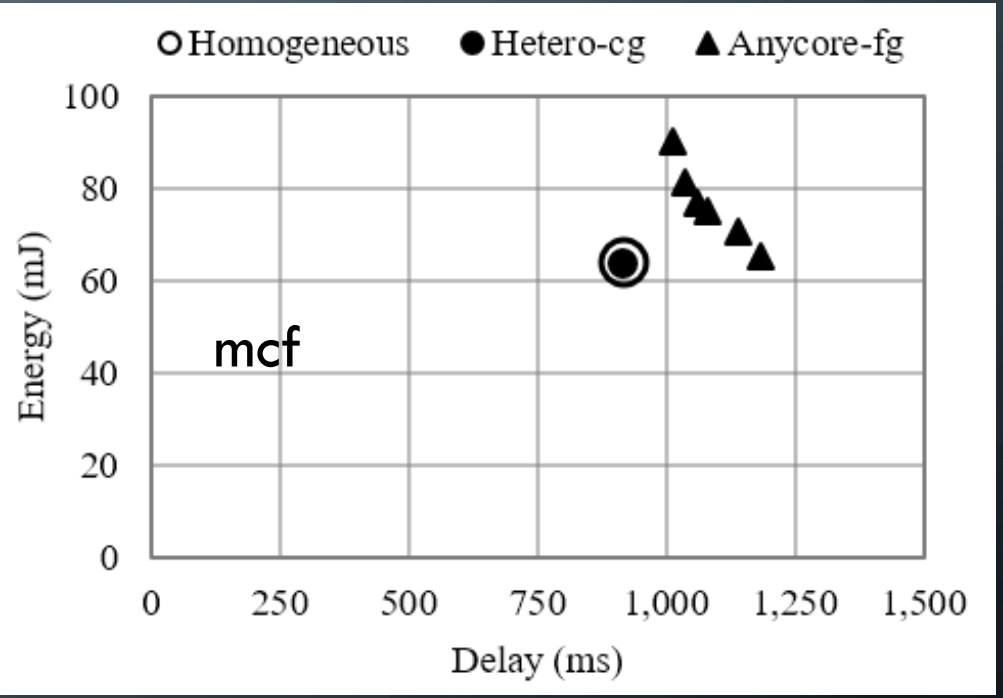
ADAPTIVE CORE VS. HETEROGENEOUS MULTICORE

- Highest weighted 100M SimPoints from 15 SPEC2006 benchmarks
- Customize cores to benchmarks to form a palette
- Performance obtained using C++ microarchitecture simulator
- Energy and cycle time from AnyCore PAT tool
- Compare three architectures:
  - *Homogeneous*: Core yielding best harmonic-mean BIPS
  - *Hetero-cg*: Coarse-grained scheduling on customized cores
  - *AnyCore-fg*: Fine-grained scheduling on AnyCore

ADAPTIVE CORE VS. HETEROGENEOUS MULTICORE



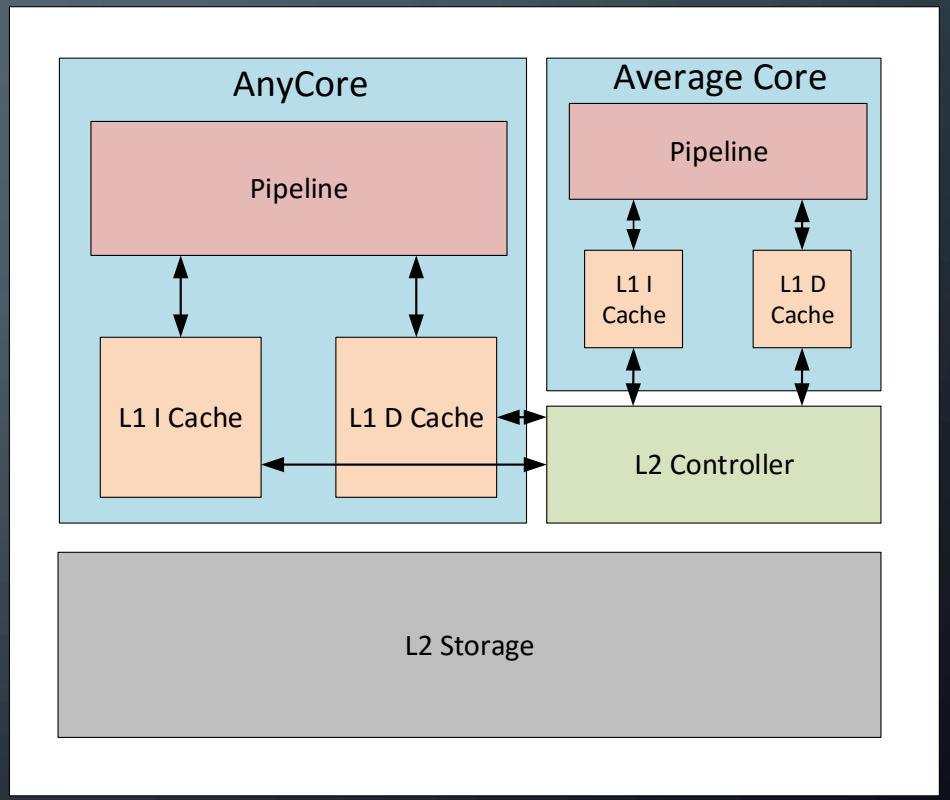


namd: AnyCore-fg is not eclipsed by either the average core (homogeneous) or the customized core

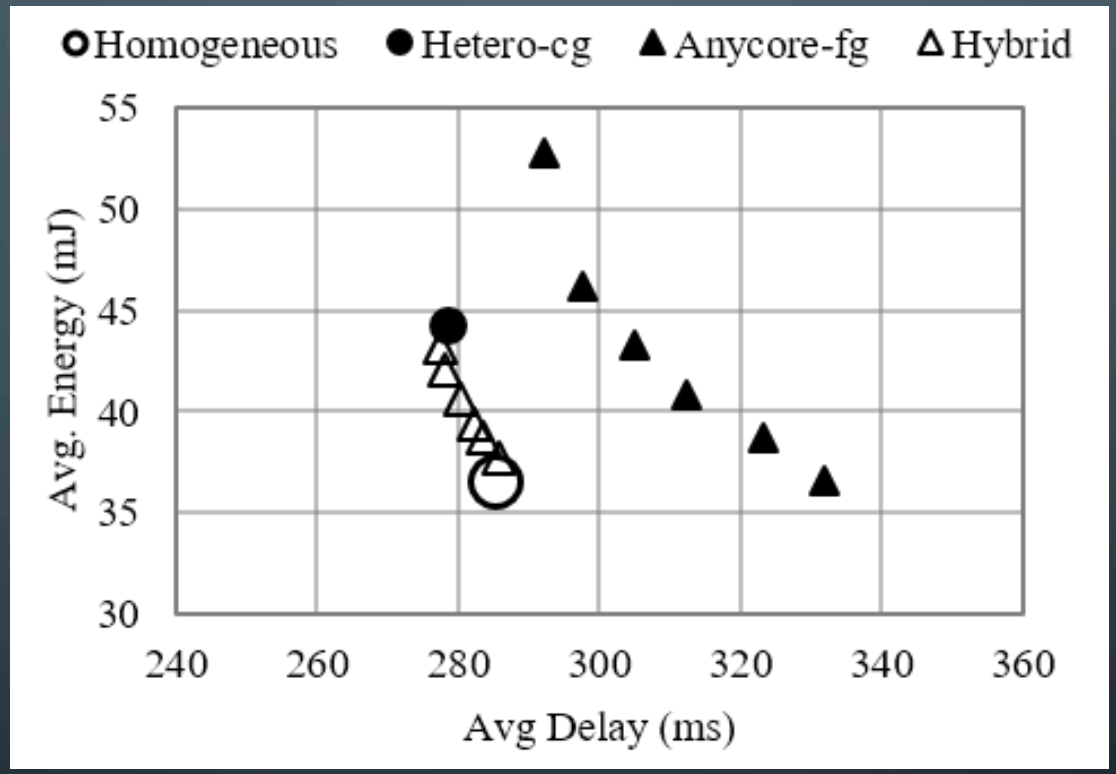
mcf: Average core eclipses Anycore-fg due to large circuit-level overheads and low phase diversity

HYBRID ARCHITECTURE

- One AnyCore + One Average Core
- Hierarchical scheduling
  - Benchmarks that favor average core, run on it for their entirety
  - Benchmarks that favor AnyCore, run on AnyCore with fine-grain scheduling



PERFORMANCE WITH HYBRID ARCHITECTURE



Key point: Hybrid is not completely eclipsed by any other type

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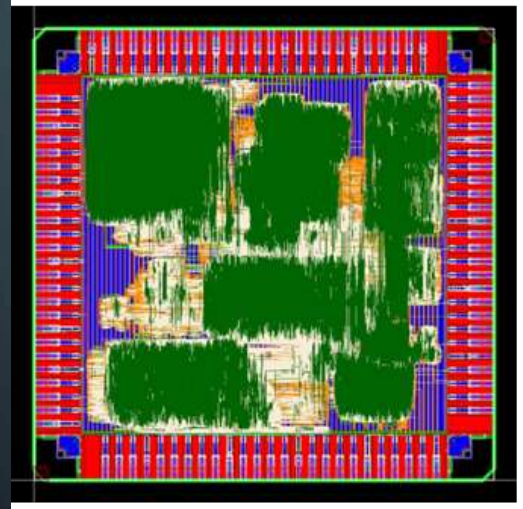
ANYCORE CHIP

- Fabricated with 130nm technology
- Dynamic energy saving techniques
  - Partition-level clock gating
  - Input gating of de-configured ports
- No power gating
  - Very low leakage at 130nm
  - Absence of power gating cells in library
- Many performance counters for experiments
- Includes neat debug features

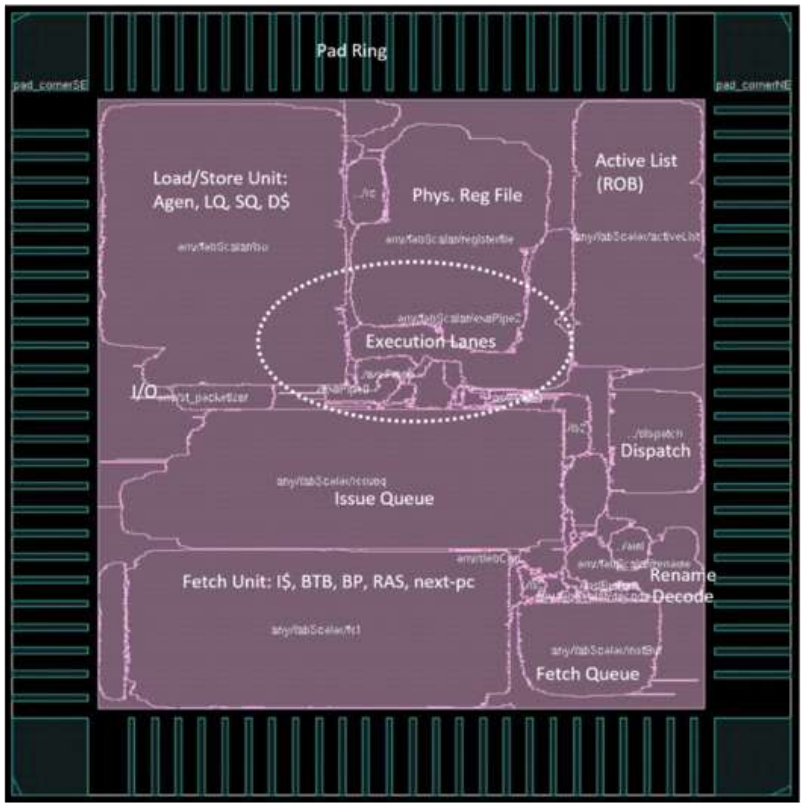
Parameter	Max Size	Allowed Configs
Fetch Width	4	1,2,3,4
Issue Width	5	3,4,5
Issue Queue	64	16, 32, 48, 64
LQ/SQ	32	16,32
PRF	128	64, 96, 128
ROB	128	64, 96, 128

ANYCORE CHIP: LAYOUT, FLOORPLAN AND PCB

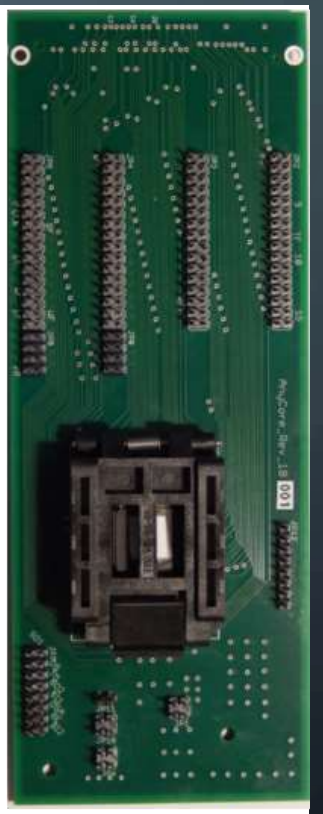
Physical design data	
Technology	IBM 8RF (130nm)
Dimensions	5 mm x 5 mm
Area	25 mm^2
Pads (signal, power)	100 (79, 21)
Transistors	3.4 million
Cells	1.5 million
Nets	7.6 million



Final Layout

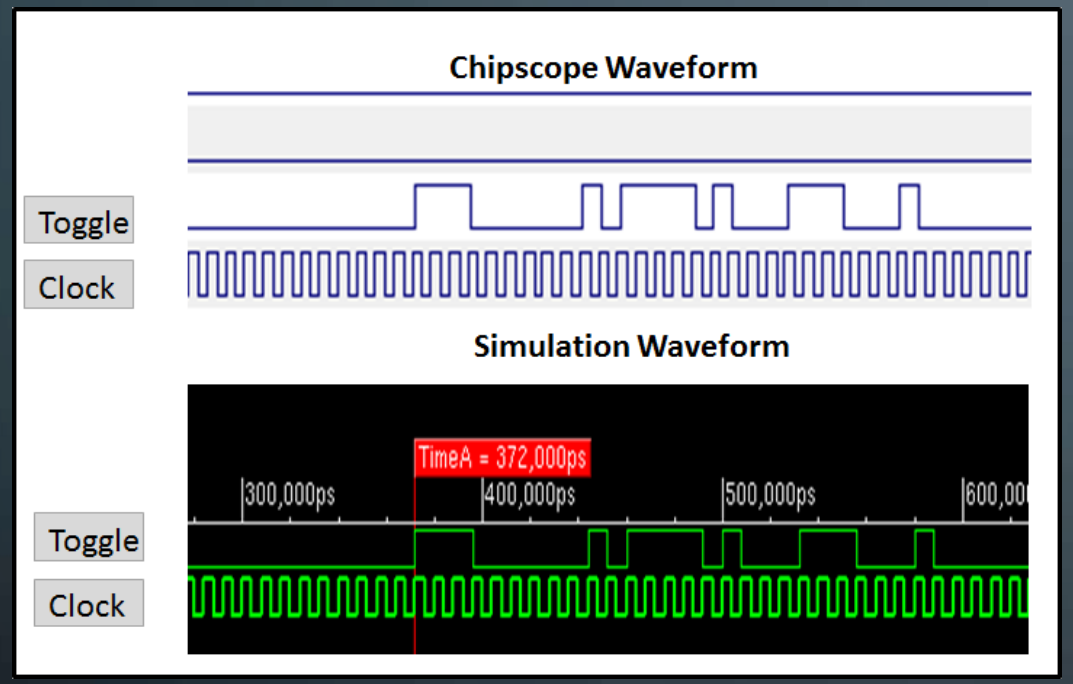


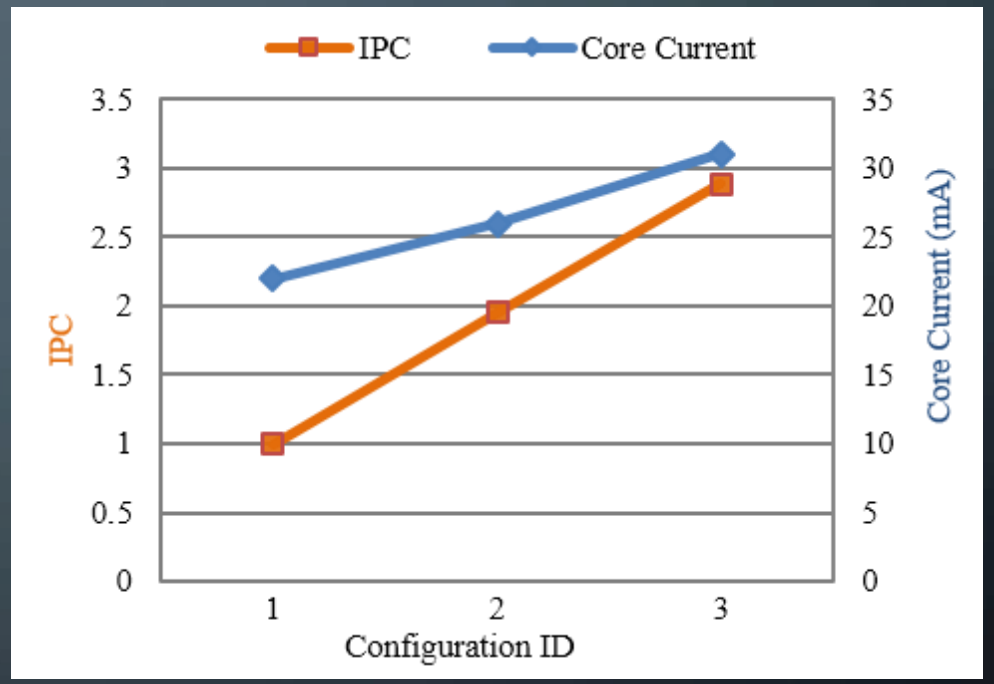
Floorplan



PCB

ANYCORE CHIP: MEASUREMENTS





Key point: Liveness test took very little effort, thanks to BIST.

Key point: Current scales with performance (resource sizes). Clock tree and synthesized caches make up a significant part of this.

SUMMARY

- AnyCore is a large step towards designing efficient adaptive cores
- Logic overheads of adaptivity are non-trivial and demand further research to reduce them
- AnyCore toolset will be released as an open-source tool and will be available for download from North Carolina State University

http://people.engr.ncsu.edu/ericro/research/anycore.htm

FUTURE WORK

- Further reduction of overheads
  - Make AnyCore "core-accurate" with respect to arbitrary fixed cores within its configuration space
  - Dynamic configurations achieve the same IPC, frequency, and energy of the corresponding fixed core
- Scheduling techniques, both predictive and reactive
- AnyCore as a general-purpose accelerator in a manycore system
- Further testing and measurement of the AnyCore chip

THANK YOU!

QUESTIONS