AnyCore-1: A Comprehensively Adaptive 4-Way Superscalar Processor

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AnyCore-1

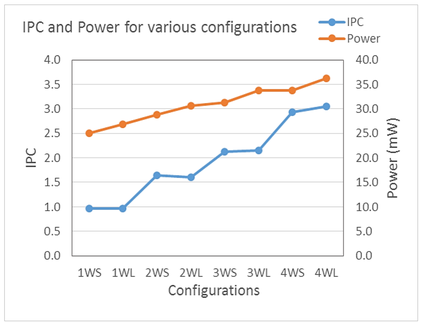
- A comprehensively adaptive out-of-order superscalar core which adapts to the available ILP in programs
- Dynamically changes superscalar width and sizes of ILP extracting structures
- Orthogonal to DVFS and can improve energy efficiency further
- To the best of our knowledge, AnyCore-1 is the first adaptive processor chip

Parameter	Max Size	Legal Configs
Fetch Width	4	1, 2, 3, 4
Issue Width	5	3, 4, 5
Issue Queue	64	16, 32, 48, 64
Load/Store Queues	32	16, 32
Phys. Register File	128	64, 96, 128
Reorder Buffer	128	64, 96, 128

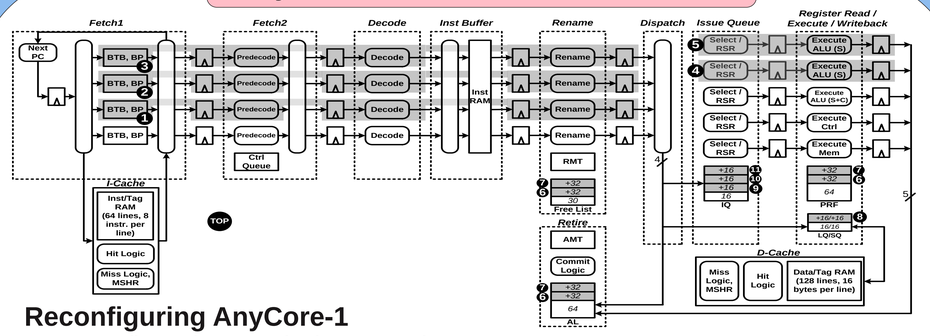
Key Results

- Power consumption and IPC scale with configured core size
- Idle power is large due to clock tree and fully synthesized caches

Power	Configuration	Power (mW)
Leakage Power	Smallest / Biggest	0.01
Idle Power	Smallest	21
Idle Power	Biggest	25

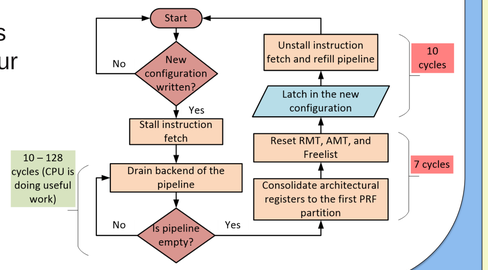


AnyCore-1 Microarchitecture



Reconfiguring AnyCore-1

- Reconfiguration penalty is ~20 cycles
- Reconfiguration can take up to 150 cycles
- Three ways to trigger reconfiguration in our test setup
  1) By the program, by issuing a store with the configuration to a reserved memory location
  2) By the testbench hardware based on performance counter driven bottleneck analysis
  3) By the console program based on scheduling constraints



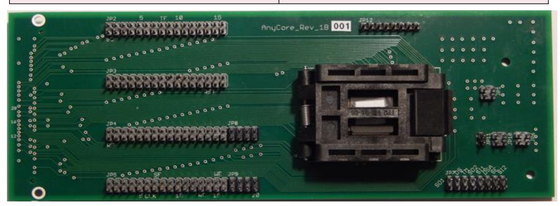
AnyCore-1 Chip Details

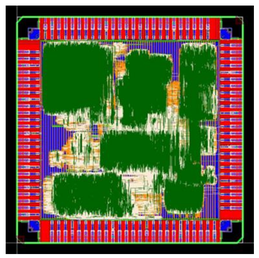
- Fabricated in 130nm technology
- Clock gating at level of lanes and structure partitions
- Input gating of de-configured ports
- CQFP-100 package (79 signal pads, 21 power pads)

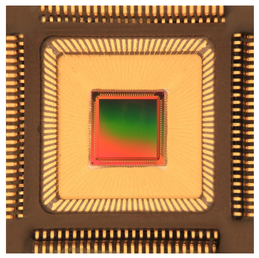
Test Infrastructure

- Xilinx ML-605 board used as a testbench
- Custom mezzanine card interfaces chip to ML605
- L2 Controller in FPGA (currently uses block RAMs)
- FPGA talks to AnyCore-1 through a **Management Bus**
- A console program running on a PC communicates with the FPGA to load benchmarks, write AnyCore-1 configurations, and read performance counters

Physical Design Information	
Technology	IBM 8RF (130nm)
Dimensions	5 mm x 5 mm
Pads (Signal, Power)	100 (79, 21)
Transistors	3.4 million
Cells	1.5 million
Nets	7.6 million







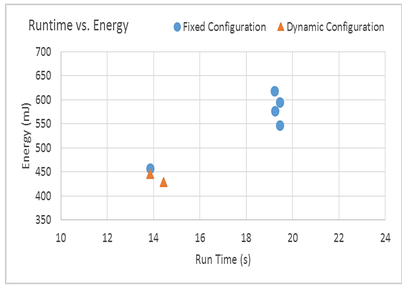
Experiments with AnyCore-1

- AnyCore-1 successfully runs many different microbenchmarks, with dynamic reconfiguration enabled and disabled
- Currently we are trying to run SPEC 2000 SimPoints on AnyCore-1

Benchmark	Dynamic Instr. (million)	Avg. IPC	Avg. Power (mW)
Reduce an array to a sum	235.46	3.05	36.25
Bubble Sort an array	36.92	0.32	27.50
Prime Number Generator	88.28	1.52	30.63
Linear Feedback Shift Register	67.11	1.57	30.63
Sum first N natural numbers	67.11	4.00	36.25

Adaptive Core vs. Fixed Cores

- Scheduler adjusts configuration for each program phase to minimize energy while maintaining close to maximum performance for the phase
- Dynamic reconfiguration at phase boundaries places AnyCore-1 at the pareto frontier
- AnyCore-1 enables the scheduler to trade performance for lower energy



References

[1] R. Basu Roy Chowdhury, A. K. Kannepalli, S. Ku, and E. Rotenberg. “AnyCore: A Synthesizable RTL Model for Exploring and Fabricating Adaptive Superscalar Cores.” ISPASS'16, pp. 214-224, April 2016.

[2] Niket K. Choudhary, Salil V. Wadhavkar, et al. “FabScalar: Composing Synthesizable RTL Designs of Arbitrary Cores Within a Canonical Superscalar Template.” ISCA-38, pp. 11-22, June 2011.

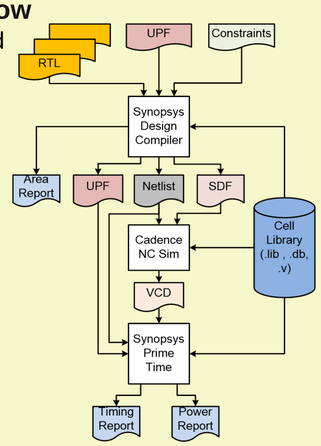
AnyCore Toolset

AnyCore RTL Design

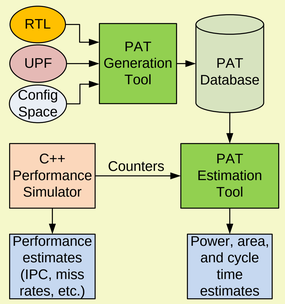
- A synthesizable parameterized RTL design of an adaptive superscalar core
- Can generate both adaptive and fixed cores of arbitrary maximum size
- The RTL is paired with UPF based power domain description for power gating of lanes and partitions

AnyCore CAD Flow

- Industry-standard synthesis and analysis flow to easily quantify circuit-level overheads
- Clock gating and power gating methodology to maximize power savings from disabled resources



AnyCore PAT Tool



- A Power-Area-Timing database generation tool that can be coupled with C++ based microarchitecture simulators for broad exploration studies
- Automatically synthesize, analyze, and populate PAT database – easy to use for computer architects who are not familiar with low-level flows
- Uses UPF-based per-domain power analysis to populate power database

Enables Adaptive Core Research

- Understand circuit-level overheads of adaptivity
- Compare comprehensively adaptive cores with other adaptive architectures such as heterogeneous multicore
- Fabricate adaptive superscalar cores like AnyCore-1

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