A 5.5 GHz Network on Chip in 45nm CMOS Process

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Introduction

Today's SOCs have a large number of components constantly communicating with each other through a fast and efficient on chip network. In this project a 3x3 Network-On-Chip was designed in a 45nm CMOS process. The design is fully pipelined with a pipeline separating the arbiter and the crossbar switch. The final design successfully operated at 5.5 GHz at 1.0V supply and had an average power of 29.5 mWatts. The system had an overall ED^2 metric of 7.95×10^{-29}.

Design Description

The design can be divided into three major parts, namely the arbiter (Fig. 1) , the crossbar switch (Fig. 2) and the pipeline registers or flip flops (Fig. 3) . The arbiter was designed using basic static CMOS gates and have been fully optimized for a 3x3 network.

The positive edge triggered dynamic TSPC D flip flop was used as it gave a good balance between delay and energy during evaluation. Some modifications were made to the original TSPC flip flop. Since the first stage and the second stage act as a positive latch, they do not effect the C-Q delay of the flip flop. So the input transistors were made VTG to reduce leakage. Also at the second stage the clock(positive edge) is the last signal to arrive. So it was kept nearest to the output to reduce the C-Q delay. The inverter at the output was skewed to get the minimum average delay.

Results

The final circuit is very fast and has good energy-delay balance. At room temperature, the pre layout circuit operated at 9.4 GHz and the post layout circuit with parasitics (C+CC) operated at 5.8 GHz. The supply voltage was 1.0 V.The circuit consumed 5.078 pJ of energy for complete simulation of the test vectors. The average power was 1.28 mWatt. The clock buffer design gave a decent rise time at the sinks. The maximum rise time was 21.64 ps. All the important physical parameters are listed in Table 1. The reduced waveform for functional correctness is shown in Figure 5.

Conclusion

References

[1] Jan M. Rabaey, Digital Integrated Circuits (Second Edition), 2003
[2] Subhasish Mitra, Stanford EE 271, 2007
[3] Mohammed Elgamel, etc. “Noise Tolerant Low Power Dynamic TSPCL D Flip Flops”, ISVLSI’02

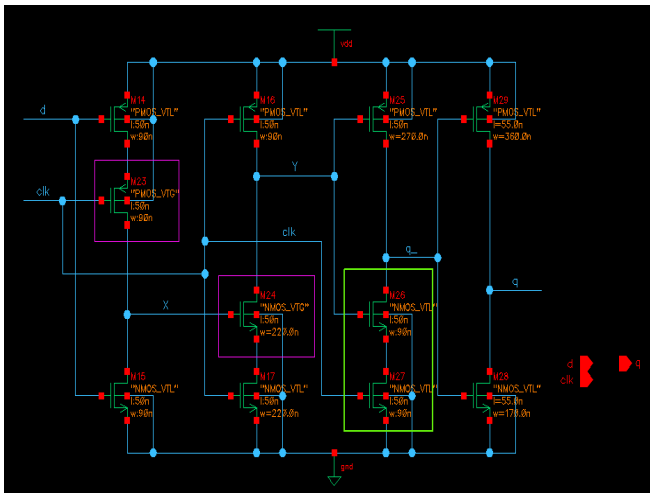

Figure 2: Flip Flop Schematic

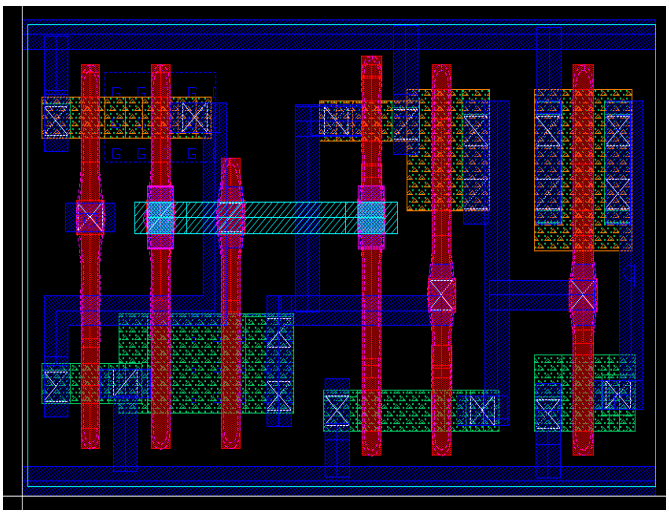

Figure 1: Flip Flop Layout With PV Bands

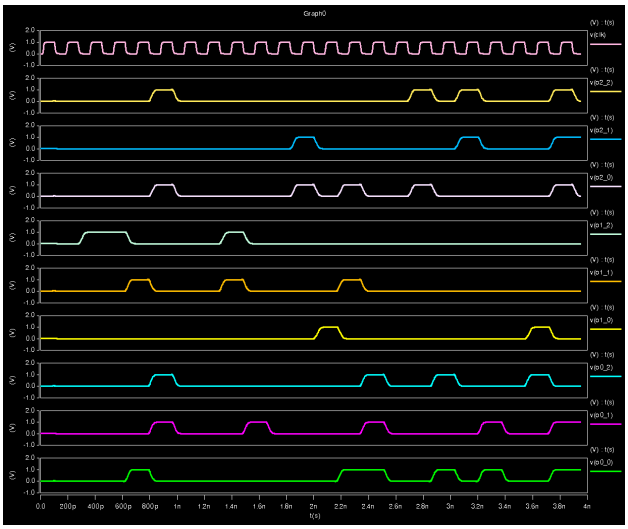

Figure 3: Output Waveforms

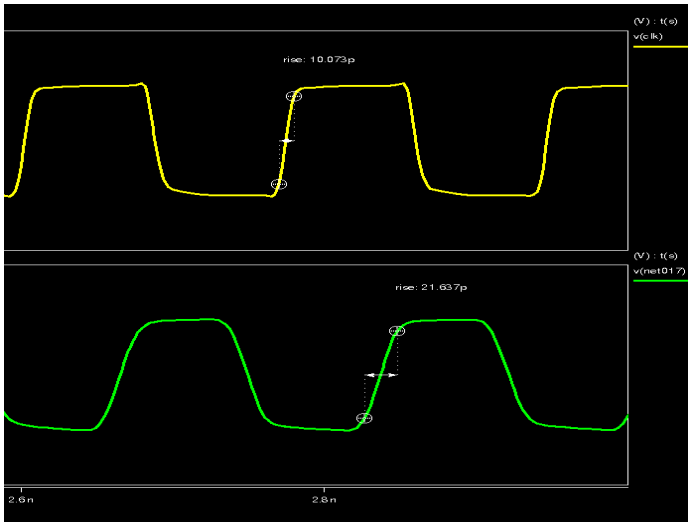

Figure 5: Clock Rise Time Analysis at Sink

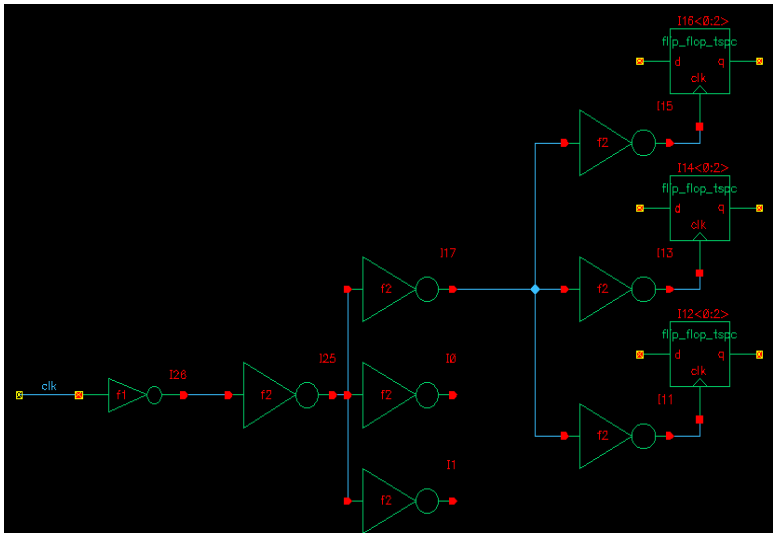

Figure 4: Clock Tree

Minimum Clock Period	**172 ps**
Supply Voltage	**1.0 V**
Energy	**5.078 pJ**
Avg. Power	**29.5 mW**
Height	**7.54 um**
Width	**13.95 um**
Area	**105.183 um^2**
No. of Transistors (Density)	**603 (5.733/um^2)**
Design Time (Total)	**100 man hours**

Table 1: Physical Parameters

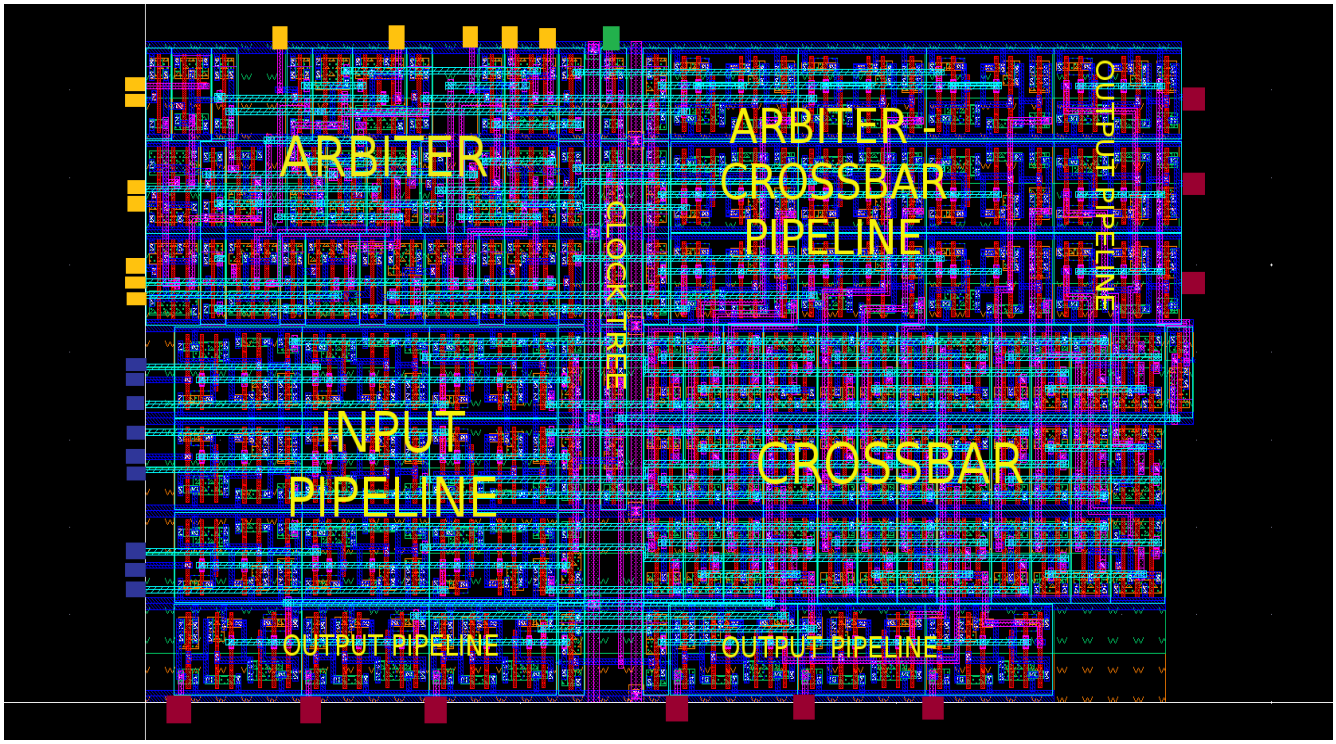

Figure 6: Final Layout

Name	Tasks
Karthik Shenoy	**Arbiter Design & Layout , Top Level Integration & Layout, Top Level Simulation, Post Layout Optimizations**
Jayaganeshwar N.	**Crossbar Design & Layout, Top Level Integration & Layout, Clock Circuitry Design**
Rangeen Basu Roy Chowdhury	**Flip Flop Design & LFD Clean Layout , Final Report**

Table 2: Division of Labour Among Team Members